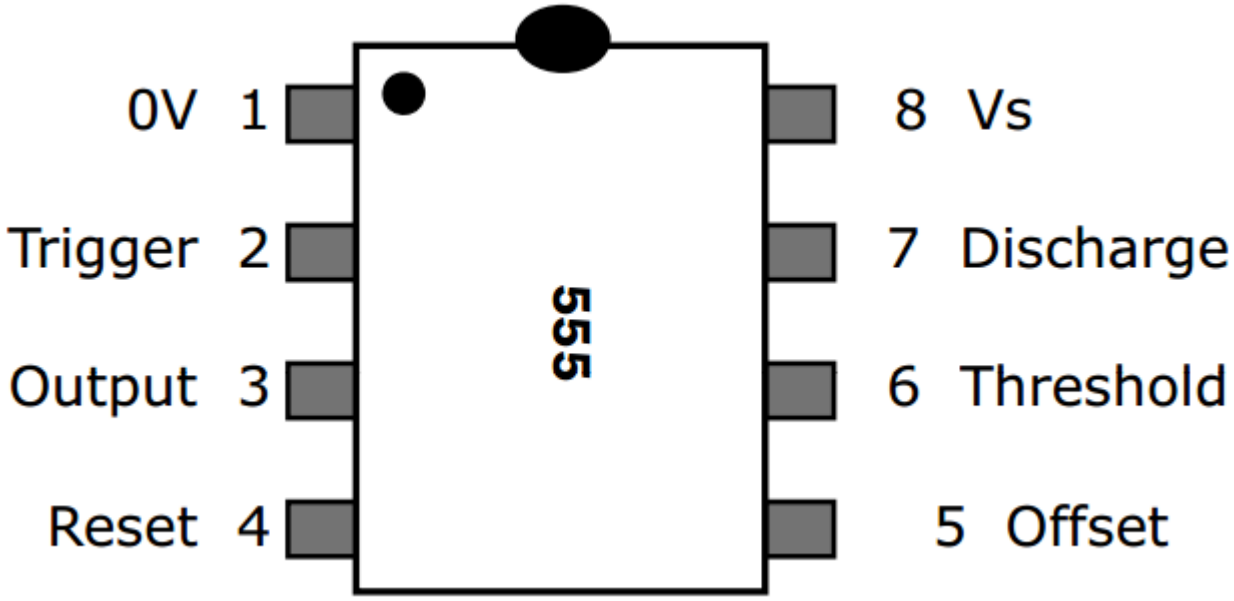
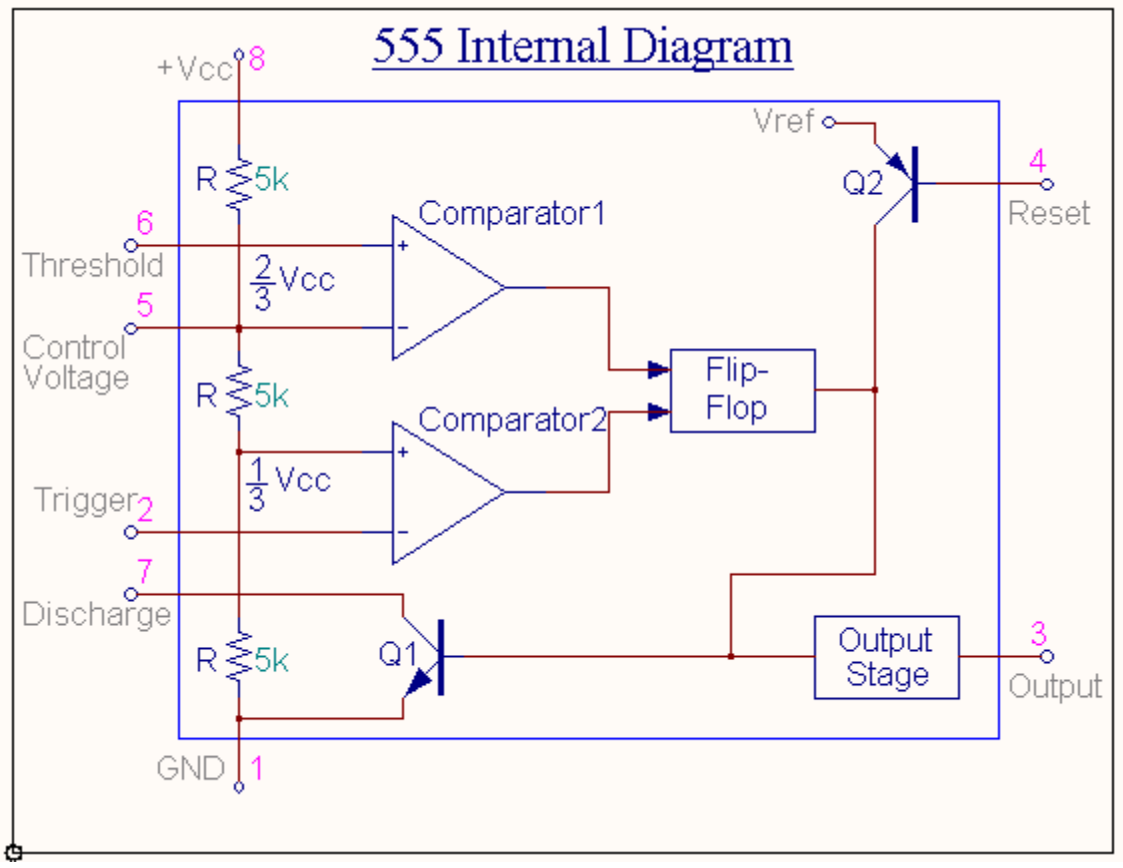
Timer 555


0V 1
Trigger 2
Output 3
Reset 4
8 Vs
7 Discharge
6 Threshold
5 Offset
555

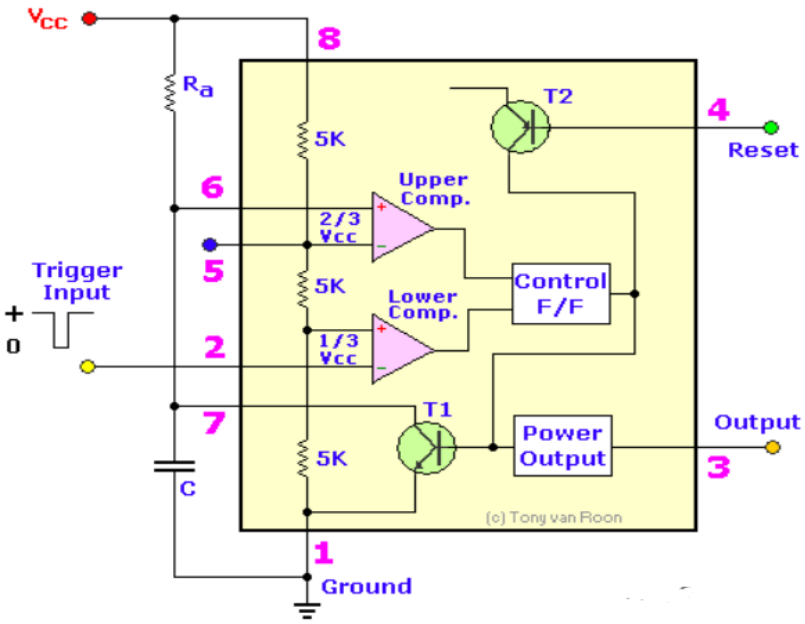
Introduction:

The 555 timer comes in a variety of number designations. The most common are NE555 and LM555. There are two modes of operation, monostable and astable. In monostable mode a single pulse with a fixed pulse width is created by means of connecting an external resistor and capacitor to the appropriate pins. The output pulse occurs after a trigger signal is sent to the timer. If different pulse widths are required the easiest way to implement this is to replace the resistor with a potentiometer. Adjust the potentiometer for the new pulse width setting and then trigger the timer. In astable mode, some times called free running, multiple pulses are produced using two external resistors and one external capacitor. The waveform has a fixed period and duty cycle. Selecting different values of resistors and the capacitor can change the period and duty cycle. No trigger signal is required for pulses to be generated in astable mode.



Definition of Pin Functions:

Pin 1 (Ground): The ground (or common) pin is the most-negative supply potential of the device, which is normally connected to circuit common (ground) when operated from positive supply voltages.



Pin 2 (Trigger): This pin is the input to the lower comparator and is used to set the latch, which in turn causes the output to go high. This is the beginning of the timing sequence in monostable operation. Triggering is accomplished by taking the pin from above to below a voltage level of 1/3 V+ (or, in general, one-half the voltage appearing at pin 5). The action of the trigger input is level-sensitive, allowing slow rate-of-change waveforms, as well as pulses, to be used as trigger sources. The trigger pulse must be of shorter duration than the time interval determined by the external R and C. If this pin is held low longer than that, the output will remain high until the trigger input is driven high again. One precaution that should be observed with the trigger input signal is that it must not remain lower than 1/3 V+ for a period of time longer than the timing cycle. If this is allowed to happen, the timer will retrigger itself upon termination of the first output pulse. Thus, when the timer is driven in the monostable mode with input pulses longer than the desired output pulse width, the input trigger should effectively be shortened by differentiation. The minimum-allowable pulse width for triggering is somewhat dependent upon pulse level, but in general if it is greater than the 1uS (micro-Second), triggering will be reliable. A second precaution with respect to the trigger input concerns storage time in the lower comparator. This portion of the circuit can exhibit normal turn-off delays of several microseconds after triggering; that is, the latch can still have a trigger input for this period of time after the trigger pulse. In practice, this means the minimum monostable output pulse width should be in the order of 10uS to prevent possible double triggering due to this effect. The voltage range that can safely be applied to the trigger pin is between V+ and ground. A dc current, termed the trigger current,

must also flow from this terminal into the external circuit. This current is typically 500nA (nano-amp) and will define the upper limit of resistance allowable from pin 2 to ground. For an astable configuration operating at V+ = 5 volts, this resistance is 3 Mega-ohm; it can be greater for higher V+ levels.

Pin 3 (Output): The output of the 555 comes from a high-current totem-pole stage made up of transistors Q20 - Q24. Transistors Q21 and Q22 provide drive for source-type loads, and their Darlington connection provides a high-state output voltage about 1.7 volts less than the V+ supply level used. Transistor Q24 provides current-sinking capability for low-state loads referred to V+ (such as typical TTL inputs). Transistor Q24 has a low saturation voltage, which allows it to interface directly, with good noise margin, when driving current-sinking logic. Exact output saturation levels vary markedly with supply voltage, however, for both high and low states. At a V+ of 5 volts, for instance, the low state Vce(sat) is typically 0.25 volts at 5 mA. Operating at 15 volts, however, it can sink 200mA if an output-low voltage level of 2 volts is allowable (power dissipation should be considered in such a case, of course). High-state level is typically 3.3 volts at V+ = 5 volts; 13.3 volts at V+ = 15 volts. Both the rise and fall times of the output waveform are quite fast, typical switching times being 100nS. The state of the output pin will always reflect the inverse of the logic state of the latch, and this fact may be seen by examining Fig. 3.Since the latch itself is not directly accessible, this relationship may be best explained in terms of latch-input trigger conditions. To trigger the output to a high condition, the trigger input is momentarily taken from a higher to a lower level. [see "Pin 2 - Trigger"]. This causes the latch to be set and the output to go high. Actuation of the lower comparator is the only manner in which the output can be placed in the high state. The output can be returned to a low state by causing the threshold to go from a lower to a higher level [see "Pin 6 - Threshold"], which resets the latch. The output can also be made to go low by taking the reset to a low state near ground [see "Pin 4 - Reset"]. The output voltage available at this pin is approximately equal to the Vcc applied to pin 8 minus 1.7V.

Pin 4 (Reset): This pin is also used to reset the latch and return the output to a low state. The reset voltage threshold level is 0.7 volt, and a sink current of 0.1mA from this pin is required to reset the device. These levels are relatively independent of operating V+ level; thus the reset input is TTL compatible for any supply voltage. The reset input is an overriding function; that is, it will force the output to a low state regardless of the state of either of the other inputs. It may thus be used to terminate an output pulse

prematurely, to gate oscillations from "on" to "off", etc. Delay time from reset to output is typically on the order of 0.5 µS, and the minimum reset pulse width is 0.5 µS. Neither of these figures is guaranteed, however, and may vary from one manufacturer to another. In short, the reset pin is used to reset the flip-flop that controls the state of output pin 3. The pin is activated when a voltage level anywhere between 0 and 0.4 volt is applied to the pin. The reset pin will force the output to go low no matter what state the other inputs to the flip-flop are in. When not used, it is recommended that the reset input be tied to V+ to avoid any possibility of false resetting.

Pin 5 (Control Voltage): This pin allows direct access to the 2/3 V+ voltage-divider point, the reference level for the upper comparator. It also allows indirect access to the lower comparator, as there is a 2:1 divider (R8 - R9) from this point to the lower-comparator reference input, Q13. Use of this terminal is the option of the user, but it does allow extreme flexibility by permitting modification of the timing period, resetting of the comparator, etc. When the 555 timer is used in a voltage-controlled mode ,its voltage-controlled operation ranges from about 1 volt less than V+ down to within 2 volts of ground (although this is not guaranteed). Voltages can be safely applied outside these limits, but they should be confined within the limits of V+ and ground for reliability. By applying a voltage to this pin, it is possible to vary the timing of the device independently of the RC network. The control voltage may be varied from 45 to 90% of the Vcc in the monostable mode, making it possible to control the width of the output pulse independently of RC. When it is used in the astable mode, the control voltage can be varied from 1.7V to the full Vcc. Varying the voltage in the astable mode will produce a frequency modulated (FM) output. In the event the control-voltage pin is not used, it is recommended that it be bypassed, to ground, with a capacitor of about 0.01uF (10nF) for immunity to noise, since it is a comparator input. This fact is not obvious in many 555 circuits since I have seen many circuits with 'no-pin-5' connected to anything, but this is the proper procedure. The small ceramic cap may eliminate false triggering.

Pin 6 (Threshold): Pin 6 is one input to the upper comparator (the other being pin 5) and is used to reset the latch, which causes the output to go low. Resetting via this terminal is accomplished by taking the terminal from below to above a voltage level of 2/3 V+ (the normal voltage on pin 5). The action of the threshold pin is level sensitive, allowing slow rate-of-change waveforms. The voltage range that can safely be applied to the threshold pin is between V+ and ground. A dc current, termed the threshold current,

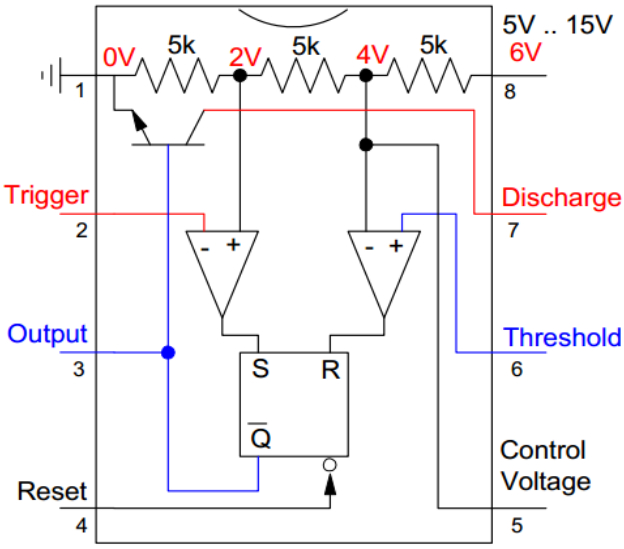
must also flow into this terminal from the external circuit. This current is typically 0.1µA, and will define the upper limit of total resistance allowable from pin 6 to V+. For either timing configuration operating at V+ = 5 volts, this resistance is 16 MΩ For 15 volt operation, the maximum value of resistance is 20 MΩ.

Pin 7 (Discharge): This pin is connected to the open collector of a NPN transistor (Q14), the emitter of which goes to ground, so that when the transistor is turned "on", pin 7 is effectively shorted to ground. Usually the timing capacitor is connected between pin 7 and ground and is discharged when the transistor turns "on". The conduction state of this transistor is identical in timing to that of the output stage. It is "on" (low resistance to ground) when the output is low and "off" (high resistance to ground) when the output is high. In both the monostable and astable time modes, this transistor switch is used to clamp the appropriate nodes of the timing network to ground. Saturation voltage is typically below 100mV (milli-Volt) for currents of 5 mA or less, and off-state leakage is about 20nA (these parameters are not specified by all manufacturers, however). Maximum collector current is internally limited by design, thereby removing restrictions on capacitor size due to peak pulse-current discharge. In certain applications, this open collector output can be used as an auxiliary output terminal, with current-sinking capability similar to the output (pin 3).

Pin 8 (V +): The V+ pin (also referred to as Vcc) is the positive supply voltage terminal of the 555 timer IC. Supply-voltage operating range for the 555 is +4.5 volts (minimum) to+16 volts (maximum), and it is specified for operation between +5 volts and + 15 volts. The device will operate essentially the same over this range of voltages without change in timing period. Actually, the most significant operational difference is the output drive capability, which increases for both current and voltage range as the supply voltage is increased.

555 Timer:

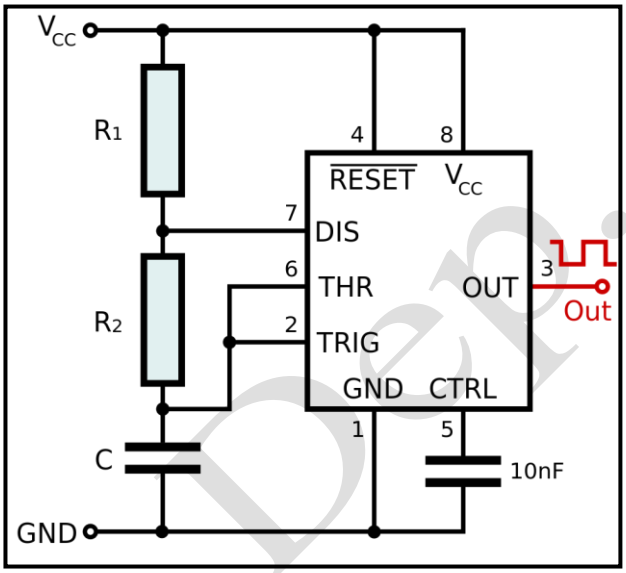
555 Timers get their name from the use of three 5k resistors in series. These resistors create two reference voltages equally spaced between ground and the power supply



The functions of the pins are as follows (assuming a 6V power supply):

- Power and Ground: self explanatory. Power can be anything from 5V to 15V.
- Trigger: When V trigger < 2V, the SR flip-flop sets and the output goes high.
- Threshold: When V threshold > 4V, the SR flip flop clears and the output goes low
- Control Voltage: Allows you to change the threshold voltage from 4V if you like
- Discharge: When the output is low, Discharge is shorted to ground through a transistor.
- Otherwise, Discharge is a floating pin.

1- Astable Operation

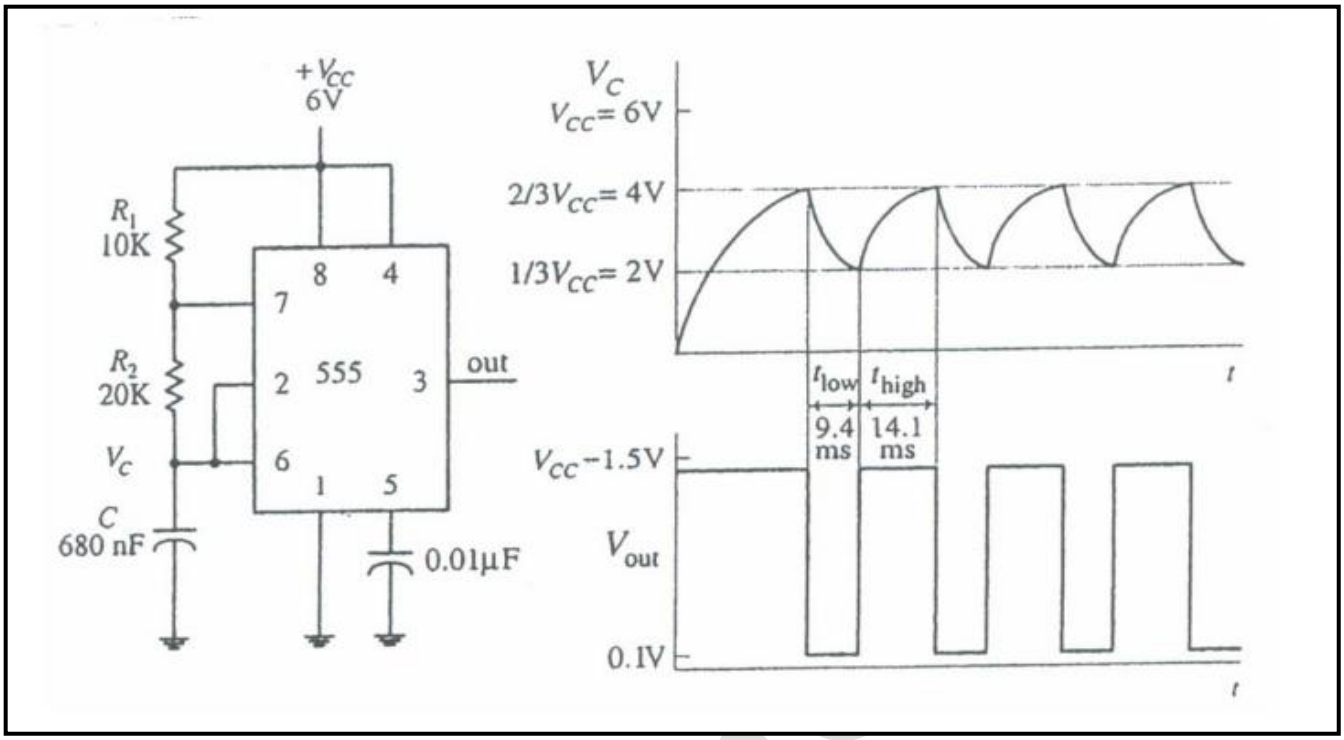


Internally the 555 timer consists of two comparators, resistors, transistors, and a digital circuit called a flip-flop (which you will study later in the course). Connecting the external resistors and capacitors as shown above results in the timer operating in the following fashion. When an applied voltage at pin 6, the threshold voltage, is > 2/3(VCC), the output at pin 3, v3, is low, that is pin 3 is at zero volts. At the same time an internally connected switch transistor that is connected between the discharge, pin 7, and ground, pin 1, is turned ON. With the discharge transistor reducing the voltage at pin 6 towards zero volts, the voltage at pin 2, the threshold voltage, is also being reduced. When the voltage at the threshold, pin 2, 2/3(V ≤ CC) then the output goes high, v3= VCC and the discharge transistor is turned OFF. When the reset voltage, pin 4 is low, the discharge transistor is turned ON. To disable the reset function connect pin 4 to VCC. Let us assume that when the timer is properly wired and initially powered, the capacitor C is initially uncharged. That means the voltage at pins 2 and6 is<2/3(VCC) and the discharge transistor is turned OFF. Consequently the output voltage at pin 3, v3, equals VCC. The capacitor then begins to charge through the R1and R2resistors and the capacitor. When the capacitor charges to a voltage level such that the voltage at pin 6,the threshold voltage, equals 2/3(VCC), the discharge transistor turns ON and the output goes to zero volts. When the capacitor discharges so that v2= v6= 1/3(VCC), the output equals VCC and the discharge transistor is OFF. The process keeps repeating until the power is turned off.

To summarize:

v2= 1/3(VCC), v3= VCC

v6= 2/3(VCC), v3= 0 volts



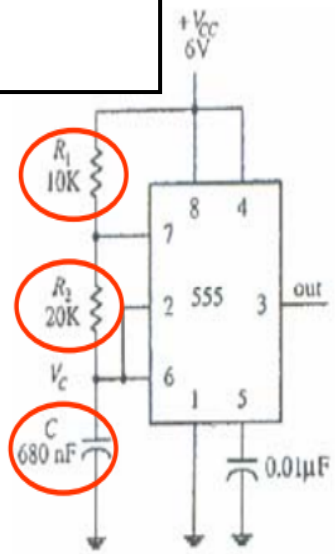
Calculation of Duty Cycle

$$t_{low} = 0.693\ R_2 C$$

$$t_{high} = 0.693\ (R_1 + R_2) C$$

$$Duty\ \ cycle = \frac{t_{high}}{t_{high} + t_{low}}$$

$$f = \frac{1}{t_{high} + t_{low}}$$



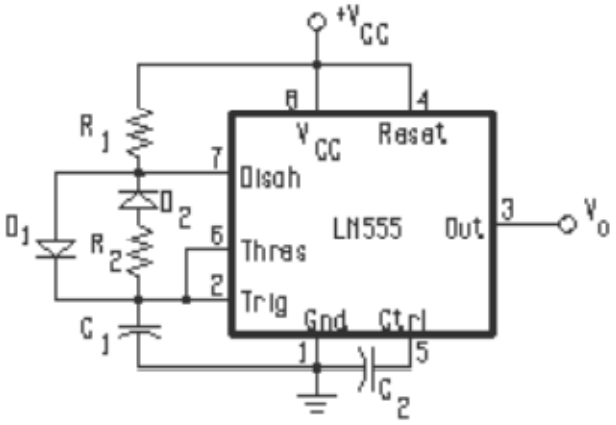
$$t_{low} = 0.693(20K)(680nF) = 9.6ms$$

$$t_{high} = 0.693(10K + 20K)(680nF) = 14.1ms$$

$$Duty\ cycle = \frac{14.1ms}{14.1ms + 9.6ms} = 0.6$$

$$f = \frac{1}{14.1ms + 9.6ms} = 42Hz$$

555 Square Wave Oscillator



$$D = \frac{R_1}{R_1 + R_2}$$

$$R_1 = \frac{D}{0.693 f_o C_1}\ ;\ R_2 = \frac{1-D}{0.693 f_o C_1}$$

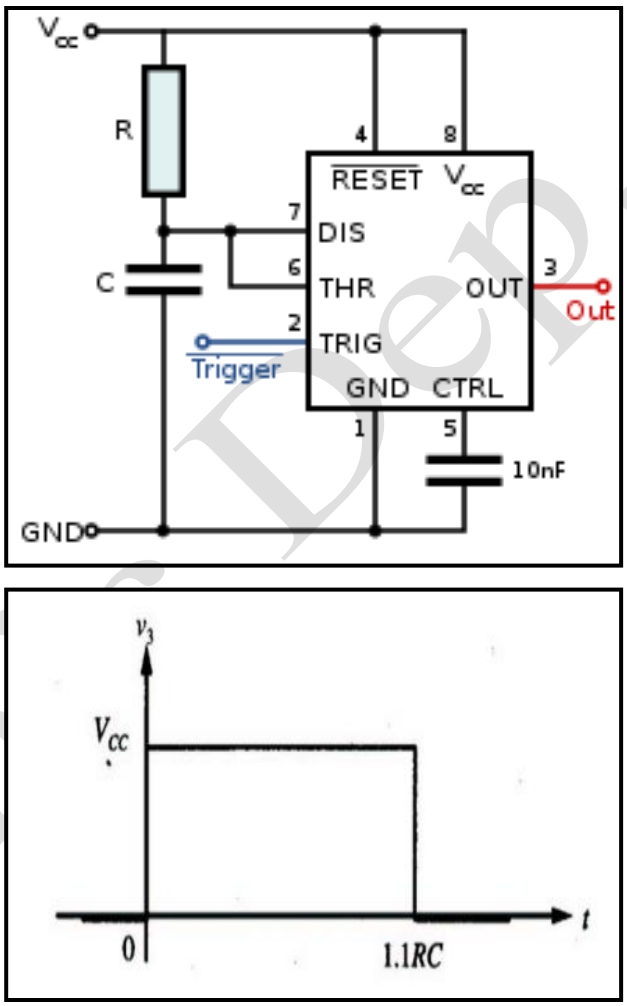
For 50% duty cycle,

$$R_1 = R_2 = \frac{1}{1.386 f_o C_1}$$

$$t_{ch} = 0.693\ R_1 C_1\ ;\ t_{disch} = 0.693\ R_2 C_1$$

$$f_o = \frac{1}{0.693(R_1 + R_2)C_1}$$

2- MONOSTABLE OPERATION



In the diagram above, pin 2, labeled v2, is the input trigger signal and pin 3, labeled v3, is the output signal. In its normal state of operation the signal at pin 2 is held to the power supply voltage, VCC. The output at pin 3 is zero volts. When the signal at pin 2 is momentarily connected to ground ,the voltage at pin 2 will become zero volts. As the voltage at pin 2 decreases and becomes < 2/3(VCC), the output at pin 3 goes high to the VCC value. When pin 3 equals VCC the internal discharge transistor turns off. The capacitor C begins to charge with a time constant of λ=RC. As the capacitor is charging the voltage at pin 6, the threshold voltage, is increasing. When the voltage at pin 6 is >2/3(VCC), the output goes to zero because the discharge transistor turns on and discharges the capacitor. For the output to go low after a trigger pulse, the trigger signal muster turn to the high, VCC state. Otherwise the output will not reset to zero volts.

To summarize:

v2< 1/3(VCC), v3= VCC

v6> 2/3(VCC), v3= 0 volts

Applications of 555 Timer

1. Astable Multivibrator
2. Monostable Multivibrator
3. Missing pulse detector
4. Linear ramp generator
5. Frequency divider
6. Pulse width modulation
7. FSK generator
8. Pulse position modulator
9. Schmitt trigger

Reference

1- Wiley - Digital Electronics - Principles, Devices and Applications (2007).

2- Internet.